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2133
#2/5-3-02
v. Jerey

PATENT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Mohammed Ali AbdEl-Halim
AbdEl-Wahid
Application No. 10/039,934

Art Unit: 2133

Filed: October 26, 2001


For: DESIGN FOR TEST OF ANALOG
MODULE SYSTEMS

Examiner: Not yet assigned

Date: April 23, 2002

CERTIFICATE OF MAILING

I hereby certify that this paper and the documents referred to as being attached or enclosed herewith are being deposited with the United States Postal Service on April 23, 2002 as First Class Mail in an envelope addressed to: COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.


Attorney for Applicant

COMMISSIONER FOR PATENTS
WASHINGTON, DC 20231

INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 C.F.R. § 1.97(b)(3)

Listed on the accompanying form PTO-1449 and enclosed herewith are several English-language documents. Applicant respectfully requests that these documents be listed as references cited on the issued patent.

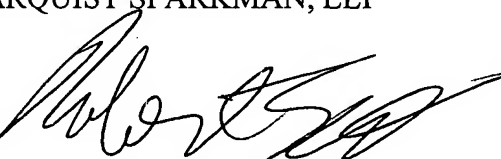
Applicant filed this Information Disclosure Statement ("IDS") before the mailing date of a first Office action on the merits. As a result, no fee should be required to file this IDS. However, if the Patent Office determines that a fee is required for Applicant to file this Information Disclosure Statement, please charge any such fees, or credit overpayment, to Deposit Account No. 02-4550. A **duplicate** copy of this Information Disclosure Statement is enclosed.

Respectfully submitted,


KLARQUIST SPARKMAN, LLP

One World Trade Center, Suite 1600
121 S.W. Salmon Street
Portland, Oregon 97204
Telephone: (503) 226-7391
Facsimile: (503) 228-9446


By



Robert F. Scotti
Registration No. 39,830

INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Docket: 1011-59137		App: 10/039,934	
				Applicant: Mohammed Ali AbdEl-Halim AbdEl-Wahid			
				Filed: October 26, 2001		Art Unit: 2133	
 PATENT DOCUMENTS							
Init.*		Number	Date	Name	Class	Sub	Filed
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			Fluence Technology Inc., "BISTMaxx™ Product Catalog," 38 p. (September 2000)				
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			LogicVision, "LogicVision - PLL BIST," 1 p. (downloaded from http://www.logicvision.com/products/pll.html on April 10, 2001)				
			Chatterjee and Nagi, "Design for Testability and Built-In Self-Test of Mixed-Signal Circuits: A Tutorial," <i>IEEE 10th Int'l Conference on VLSI Design</i> , pp. 388-92				
			Wey, "Mixed-Signal Circuit Testing -- A Review," <i>Third Int'l Conference on Electronics, Circuits and Systems</i> , pp. 1064-67 (1996)				
			Lin et al., "Automatic BIST Design Tool for Mixed-Signal Circuits," <i>AUTOTESTCON '98: IEEE Systems Readiness Technology Conference</i> , 97-102 (1998)				
			Lubaszewski et al., "Design of Self-Checking Fully Differential Circuits and Boards," <i>IEEE Transactions on VLSI Systems</i> , vol. 8, no. 2, pp. 113-28 (April 2000)				

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT			Docket: 1011-59137	App: 10/039,934	
			Applicant: Mohammed Ali AbdEl-Halim AbdEl-Wahid		
			Filed: October 26, 2001	Art Unit: 2133	
					
			"IEEE Standard for a Mixed-Signal Test Bus," <i>IEEE Std. 1149.4</i> , 84 pp. (2000)		
			"IEEE Standard Test Access Port and Boundary-Scan Architecture," <i>IEEE Std. 1149.1-1a</i> , 172 pp. (1993)		
			Nicolaidis & Zorian, "Scaling Deeper to Submicron: On-Line Testing to the Rescue," <i>IEEE Proceedings of the Design, Automation and Test in Europe Conference and Exhibition</i> , 1 p. (1999)		
			Milor, "A Tutorial Introduction to Research on Analog and Mixed-Signal Circuit Testing," <i>IEEE Transactions on Circuits and Systems--II: Analog and Digital Signal Processing</i> , vol. 45, no. 10, pp. 1389-1407 (October 1998)		
EXAMINER:			DATE		
*Examiner: Initial if considered, whether or not in conformance with MPEP 609; draw line through cite if not in conformance and not considered. Send copy.					

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